A 23-GHz Low-Noise Amplifier in SiGe Heterojunction Bipolar Technology

Gerd Schuppener[1,*], Takashi Harada[2] and Yinggang Li[3,†]

[1] Royal Institute of Technology, Dept. of Electronics, FMI, 16440 Kista, Sweden

[2] Hitachi Ltd., Device Development Center, 198-8512 Tokyo, Japan

[3] Ericsson Microwave Systems AB, MHSERC, 43184 Mölndal, Sweden

[†] Corresponding author, Email: Yinggang.Li@EMW.Ericsson.se

Abstract **- A monolithic low-noise amplifier for operation in the 23-GHz band is presented. The circuit has been designed utilizing an advanced 0.2-micron SiGe heterojunction bipolar technology, featuring npn transistors with f_T and f_{max} of about 90- and 100-GHz, respectively. Measurements show a gain of 21-dB and noise figure of 4.1-dB at 23-GHz, which compare reasonably well with simulated results. The circuit consumes 20-mA from a 2.5-V single supply. To our knowledge, 23 GHz band is the highest operation frequency reported so far for LNA in SiGe technology.**

I. INTRODUCTION

The rapid increase of multimedia services and the liberalization of the telecommunication market have created demands for broadband wireless systems. A well-designed wireless access system reduces the need of a complex, fixed infrastructure. Moreover, it offers flexible connection capacity that can dynamically be adapted to the immediate needs of the end-user, thus providing a cost-efficient solution. Public broadband services over radio, however, require bandwidth that is available only at relatively high microwave frequencies. To exploit today's microwave radio communication links for this kind of application the required radio transceiver hardware has to be implemented using low-cost, low-power IC technologies, where Si-based technologies are desirable candidates.

Recent publications describe complex transceiver circuits using Si or SiGe bipolar technologies for frequencies up to 5.8-GHz [1]-[3] and components of a RF front-end for frequencies up to 11-GHz [4]-[8]. Low-noise amplifier (LNA) is a key component in the receiver-end. Earlier LNA work using SiGe technologies has revealed promising gain and noise-figure (NF) performances [9]. Most of them, however, aimed at frequencies below 6 GHz. At higher frequencies, LNA with 26-dB gain and 2-dB NF was impressively obtained at 10.5 GHz. The 16-GHz LNA [10], which to our knowledge is the highest frequency reported so far for SiGe LNAs, demonstrated a 4-dB noise figure and 8-dB gain.

To further exploit the potential of SiGe technology for applications at even higher frequencies, we have investigated LNAs in Hitachi's SiGe-HBT technology for frequencies ranging from 5 to 38 GHz. This paper describes the LNA for 23 GHz which is one of the frequency bands used today in line-of-sight telecommunication systems.

II. DEVICES AND TECHNOLOGY

Hitachi's SiGe-HBT technology, utilized here, is based on trench isolated npn-transistors with minimum drawn-emitter size of 0.2x1 μm^2 and f_T and f_{MAX} of about 90 and 100 GHz, respectively [11]. The devices exhibit a DC-current gain of about 150 and are modelled using standard Gummel-Poon model. For passive elements, the technology offers poly-Si based resistors with various sheet resistivities, MIM capacitor of 0.7fF/μm^2 and 4 layers of interconnect, with an option to increase the thickness of the topmost metal layer.

Recent development in Hitachi's SiGe HBT/CMOS technology was based on SOI on high-resistivity

[*] Present address: Maxim Integrated Products, Design Center Hanover, 30625 Hanover, Germany

0-7803-6540-2/01/$10.00 (C) 2001 IEEE

substrate and has revealed a 180-GHz f_{max} and 76-GHz f_t. High-quality passive elements are achieved also by using the high-resistivity substrate [12].

III. Low-Noise Amplifier Design

The design of an LNA involves numerous tradeoffs. The amplifier must have sufficient gain to overcome mixer noise contribution, but should not be so much to cause mixer overload. Good noise characteristics are desired while accomplish input and output matching. Additionally, the non-linear performance must be adequate to ensure sufficient dynamic range of the receiver.

A. Amplifier Topology

As initial simulations indicated, a single common emitter (CE) amplifier will not be sufficient to provide the gain required to overcome the NF of successive receiver stages. Furthermore, the noise figure of the transistor is already relatively high at the frequency of interest so that the influence of additional circuitry must be kept low. Therefore, a cascade of two inductively loaded CE stages which were both optimized for low noise was chosen. The first stage also uses inductive emitter degeneration which improves matching and linearity [8].

In a radio receiver, an LNA is commonly followed by a mixer which is a non-linear device whose input impedance will change when modulated with the local oscillator signal. In order to de-sensitize the LNA from load changes we have used an emitter follower as output stage.

Each of the CE stages has its own base current bias which can be adjusted through pads. Bias and supply voltages have been de-coupled with on-chip capacitors. The circuit schematic is shown in Fig.1.

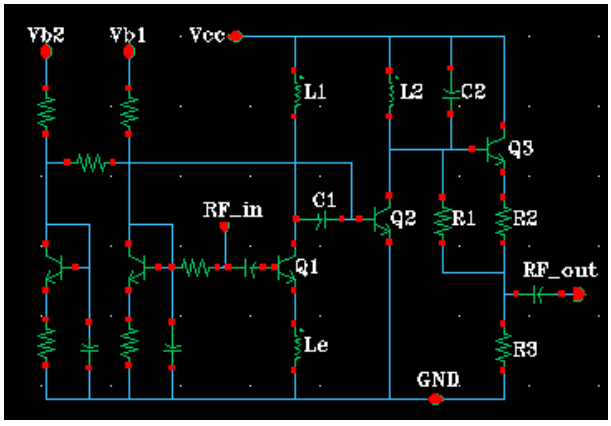

Fig. 1. Simplified schematic for the LNA.

Since the circuit is to be evaluated on-chip, no package parasitics have been taken into account during this design phase.

B. Amplifier Optimization

The transistors noise parameters, minimum noise figure, F_{min}, and optimum source impedance, Z_{Sopt}, in dependence of the collector current density have been extracted from simulated y-parameters with the method described in [13]. In conventional MMIC design, impedance matching networks are used to transform the impedance at the system interface - commonly 50-Ω - to the optimum source impedance of the device. However, using Si substrates, high-Q matching networks are difficult to realize. Instead, transistor device geometry is optimized to achieve noise and impedance match.

After the minimum noise figure has been determined, the emitter length is scaled to yield an optimum source resistance of 50-Ω. In the used technology, however, the emitter sizes cannot be freely chosen, but a set of device sizes is available only. The closest match, with R_{Sopt} about 45-Ω resulting in an optimum source resistance slightly lower than desired, was achieved by connecting three transistors with 0.2x4-μm^2 emitter area each in parallel. Biased at a collector current of 2.9-mA the transistor array offered minimum noise figure of approximately 2.6-dB. The same array with identical biasing is used for both CE stages. In order to match the input impedance of the LNA to 50-Ω, the first stage uses inductive emitter degeneration which increases the input resistance by $2pf_TL_e$. Due to the feedback at high frequencies the linearity is improved as well. The required inductance value is about 160-pH which is well suited for on-chip integration.

Input matching of the second stage is optimized using load inductance L_1 in conjunction with the interstage ac-coupling capacitance C_1. The load of this stage, which is formed by the parallel resonance of inductor L_2, capacitor C_2 and the base-collector junction capacitance of Q_3, has been tuned to the frequency of interest.

The emitter follower uses an array of five transistors with 0.2x4-μm^2 emitter area each in parallel. The emitter follower is biased at higher current to ensure linearity and 50-Ω output matching. With 2.5-V supply voltage the collector current is 6-mA. The emitter follower uses resistive feedback R_1, R_2, to stabilize the output stage at frequencies around 18-GHz.

C. Inductor Modeling

The circuit performance strongly relies on the three on-chip square-spiral inductors, thus, the accuracy of the model is crucial for the design. Often, models for on-chip inductors are derived from and fitted to data from earlier process runs. Here, no such data was available and hence, the inductors have been carefully developed using different simulation tools. Additionally, strong tuning of the amplifier structure was avoided to make the design less sensitive to modeling uncertainties.

First, the coarse value of the inductor was estimated using microwave design tool HP EEsof. Next, the physical dimensions of the inductors were extracted and optimized using both EEsof built-in inductor models and software tool Asitic [14]. Finally, the inductor layout was verified with field simulator Momentum.

Four metal layers are available in the process. The topmost metal, which is also the thickest, was used for the spiral inductors to diminish conductor losses and substrate impact.

IV. Results

The microphotograph of the LNA chip is shown in Fig. 2. The circuit was probed by Picoprobe 40GHz GSG-probes on Cascade Summit 11000 probe-station. The measurement of the transducer power gain was performed using HP 85107B Vector Network Analyzer (VNA). Calibrations were performed using SOLT (Short-Open-Line through-Termination) configuration on Alumina substrate.

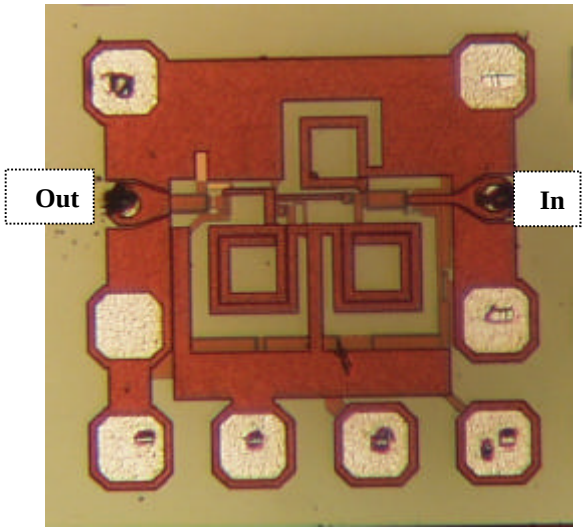

Fig. 2 The microphotograph of the LNA chip

The noise figure was measured using a noise source, a mixer, a LO signal source and a NF-meter. The gain was also monitored on the NF-meter and the results corresponded fairly with the S-parameter measurement on the VNA.

Figure 3 shows the measured gain and NF, together with the expected results from simulation. Measured gain of 21 dB and NF of 4.1 dB at 23 GHz were achieved. In view of the fact that no inductor models were available and no full-wave simulator was used either for inductor design, the agreement of the measured and simulated gain should be regarded as satisfactory at this first try. The measured noise figure, however, is about half-dB higher than expected from simulation.

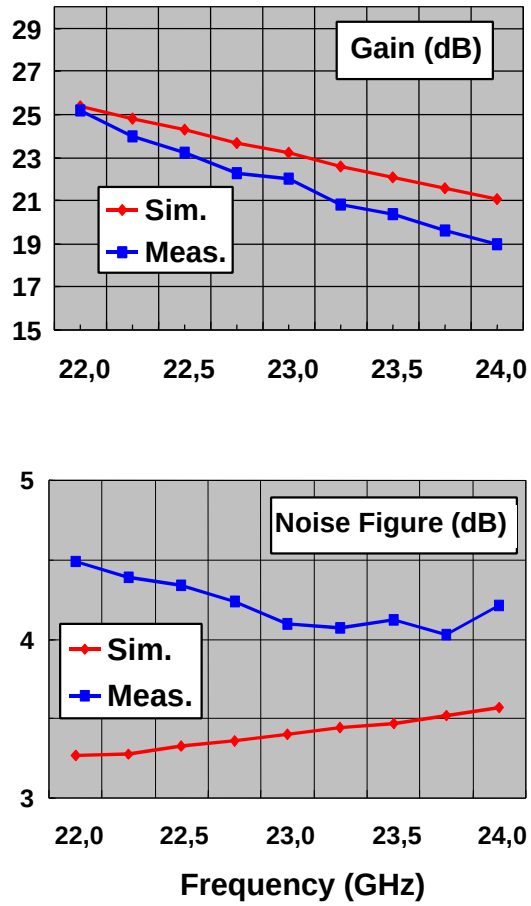

Fig. 3 Measured and simulated transducer power gain (upper) and the noise-figure (lower) of the LNAs, all 50-Ω referred.

V. CONCLUSIONS

A low-noise amplifier for usage in microwave radio links with carrier frequency of 23-GHz has been investigated. The circuit is implemented in a SiGe-HBT technology and has demonstrated a gain of 21 dB and a noise figure of 4.1dB at the frequency.

The obtained results suggest that monolithic integration of key radio front-end circuits in advanced Si-based technologies is feasible even at microwave frequencies as high as above 20 GHz.

ACKNOWLEDGMENTS

The authors would like to thank Dr. Bertil Hansson and Dr. Ola Tageman for their assistance with measurement. We gratefully acknowledge Dr. Katsuyoshi Washio, Dr. Mehran Mokhtari and Dr. Boris Kerzar for fruitful discussions and their support.

REFERENCES

[1] J. R. Long, "A low-voltage 5.1-5.8 Ghz image-reject downconverter RF IC", *IEEE Journal Solid-State Circuits*, vol. 35, no. 9, pp. 1320-1328, September 2000.

[2] M. A. Copeland, S. P. Voinigescu, D. Marchesan, P. Popescu, and M.C. Maliepaard, "5-GHz SiGe HBT monolithic radio transceiver with tunable filtering," *IEEE Trans. Microwave Theory and Tech.*, vol.. 48, no. 2, pp. 170-181, 2000.

[3] M. Madihian, T. Drenski, L. Desclos, H. Yoshida, H. Hirabayashi, and T. Yamazaki, "A 5-GHz-band multifunctional BiCMOS Transceiver Chip for GMSK modulation wireless systems," *IEEE Journal Solid-State Circuits*, vol. 34, no. 1, pp. 25-32, January 1999.

[4] M. Soyuer, J.-O. Plouchart, H. Ainspan and J. Burghartz, "A 5.8-GHz 1-V low-noise amplifier in SiGe bipolar technology," *IEEE RF Integrated Circuits Symposium*, pp. 19-22, 1997.

[5] H. Ainspan, M. Soyuer, J.-O. Plouchart and J. Burghartz, "A 6.25 GHz low DC power low-noise amplifier in SiGe," *IEEE Custom Integrated Circuits Conference*, pp.177-180, 1997.

[6] U. Erben, H. Schumacher, A. Schüppen, H. Dietrich, and J. Arndt, "Application of a production ready SiGe HBT process to 1.9, 5.7 and 10 Ghz low-noise MMICs," *Silicon Monolithic Integrated Circuits in RF Systems - Dig. Of Papers*, pp. 100-104, 1998.

[7] U. Erben, H. Schumacher, A. Schüppen and J. Arndt, "Application of SiGe heterojuncion bipolar transistors in 5.8 and 10 GHz low-noise amplifiers," *Electronics Letts*., vol. 34, no. 15, pp. 1498-1500, July, 1998.

[8] D. Zöschg, W. Wilhelm, T. F. Meister, H. Knapp, H.-D. Wohlmuth, K. Aufinger, M. Wurzer, J. Böck, H. Schäfer and A. Scholtz, "2dB noise figure, 10.5GHz LNA using SiGe bipolar technology," *Electronics Letts.*, Vol. 35, no.25, pp. 2195-2196, Dec. 1999

[9] D. Zöschg, W. Wilhelm, H. Knapp, K. Aufinger, J. Böck, T. F. Meister, M. Wurzer, H.-D. Wohlmuth, and A. L. Scholtz, "Monolithic low-noise amplifiers up to 10 GHz in Silicon and SiGe bipolar technologies," *Proceedings of The European Microwave Conference*, Dec. 2-6, Paris, 2000.

[10] K.-B. Schad, U. Erben, E. Soenmez, P. Abele and H. Schumacher, "A Ku band SiGe low noise amplifier," **.,** *Proc. of 2000 Topical Meeting on Si Monolithic ICs in RF Systems*, Garmisch, Germany, pp. 52-54, April, 2000

[11] K. Washio, M. Kondo, E. Ohue, K. Oda, R. Kayami, M. Tanabe, N. Shimamoto, and T. Harada, "A 0.2mm self-aligned SiGe HBT featuring 107-GHz fmax and 6.7-ps ECL," *IEEE Proc. Int. Electron Device Meeting*, pp. 557-560, December 1999.

[12] K. Washio, E. Ohue, H. Shimamoto, K. Oda, R. Hayami, Y. Kiyota, M. Tanabe, M. Kondo, T. Hashimoto, and T. Harada, "A 0.2-µm 180-GHz-f_{max} 6.7-ps-ECL SOI/HRS self-aligned SEG SiGe HBT/CMOS technology for microwave and high-speed digital applications", *IEEE Proc. Int. Electron Device Meeting*, December 2000.

[13] S. P. Voinigescu, M. C. Maliepaard, M. Schröter, P. Schvan, and D. L. Harame, "A scalable high frequency noise model for bipolar transistors with application to optimal transistor sizing for low-noise amplifier design", *IEEE Proc. Bipolar Circuits and Technology Meeting*, pp. 61-64, September 1996.

[14] A. M. Niknejad, and R. G. Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RF IC's", *IEEE Journal Solid-State Circuits*, vol. 33, no. 10, pp. 1470-1481, October 1998 .